In the Claims:

1 (previously presented): A method of grouping cells in an integrated circuit design comprising steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for a common signal domain in the integrated circuit design;

(c) selecting a cell belonging to a common signal domain that is not included in a corresponding list of cells for a common signal domain;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net in the corresponding list of cells for the common signal domain associated with the signal driver.

2 (previously presented): The method of Claim 1 further comprising a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to a common signal domain has been inserted in a corresponding list of cells for the common signal domain.

3 (previously presented): The method of Claim 2 further comprising a step of generating as output a corresponding list of cells for a common signal domain in the integrated circuit design.

4 (currently amended): The method of Claim 1 wherein step (e) [[(d)]] includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

5 (previously presented): The method of Claim 1 comprising performing steps (b), (c), (d), (e), (f), and (g) for cells that are flip-flops in a scan chain.

6 (previously presented): The method of Claim 5 comprising performing steps (b), (c), (d), (e), (f), and (g) for a common signal domain that is a scan clock domain.

7 (previously presented): The method of Claim 6 comprising performing steps (d), (e), (f), and (g) for a net that is a clock net.

8 (previously presented): The method of Claim 7 comprising performing steps (d), (e), (f), and (g) for an input port that is a clock port.

9 (previously presented): The method of Claim 8 comprising performing steps (d), (e), (f), and (g) for a signal driver that is a clock driver.

10 (previously presented): A computer program product for grouping scan flops for scan testing comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a representation of an integrated

circuit design;

(b) initializing a corresponding list of cells for a common signal domain in the integrated circuit design;

(c) selecting a cell belonging to a common signal domain that is not included in a corresponding list of cells for a common signal domain;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net in the corresponding list of cells for the common signal domain associated with the signal driver.

11 (previously presented): The computer program product of Claim 10 further causing the computer to perform a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to a common signal domain has been inserted in a corresponding list of cells for the common signal domain.

12 (previously presented): The computer program product of Claim 11 further causing the computer to perform a step of generating as output a corresponding list of cells for a common signal domain in the integrated circuit design.

13 (currently amended): The computer program product of Claim 10 wherein step (e) [[(d)]] includes storing a name of the selected cell in the corresponding list of cells

for the common signal domain associated with the signal driver.

14 (previously presented): The computer program product of Claim 10 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for cells that are flip-flops in a scan chain.

15 (previously presented): The computer program product of Claim 14 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for a common signal domain that is a scan clock domain.

16 (previously presented): The computer program product of Claim 15 further causing the computer to perform steps (d), (e), (f), and (g) for a net that is a clock net.

17 (previously presented): The computer program product of Claim 16 further causing the computer to perform steps (d), (e), (f), and (g) for an input port that is a clock port.

18 (previously presented): The computer program product of Claim 17 further causing the computer to perform steps (d), (e), (f), and (g) for a signal driver that is a clock driver.